

**WHAT IS CLAIMED IS:**

1        1. A method of acquiring timing associated with an input data stream,  
2 comprising:  
3            detecting whether transitions of the input data stream fall into a predetermined  
4            portion of a sample clock period of a sample clock utilized to sample  
5            the input data stream; and  
6            evaluating whether a phase-locked loop (PLL) has acquired the timing of the  
7            input data stream according to occurrence of transitions of the input  
8            data stream in the predetermined portion of the sample clock period.

1        2. The method as recited in claim 1 wherein the evaluating further  
2 comprises determining over a plurality of time periods, each of the time periods  
3 including an increasing number of evaluation intervals, whether the PLL is locked to  
4 the timing of the input data stream according to a number of evaluation intervals  
5 having one or more transitions in the predetermined portion of the sample clock  
6 period.

1        3. The method as recited in claim 1, wherein the sample clock is a clock  
2 recovered from the input data stream.

1        4. The method as recited in claim 1, wherein the evaluating includes  
2 counting a number of evaluation intervals that have at least one transition in the  
3 predetermined portion of the clock period, generating a count indicative thereof and  
4 determining if lock is achieved according to the count.

1        5. The method as recited in claim 4 wherein the evaluation intervals are at  
2 least as long as a minimum period of frequency offset.

1        6. The method as recited in claim 4, further comprising comparing the  
2 count to a threshold count to determine if lock is achieved.

1           7.     The method as recited in claim 4, further comprising adjusting an  
2     output frequency of a variable frequency oscillator circuit if it is determined that lock  
3     is not achieved.

1           8.     The method as recited in claim 7, wherein the output frequency is  
2     adjusted by changing a variable impedance associated with the oscillator circuit until  
3     lock is achieved.

1           9.     The method as recited in claim 8 wherein the variable impedance is  
2     changed by adjusting at least a portion of the variable impedance in increasing  
3     increments around an initial impedance value.

1           10.    The method as recited in claim 9 further comprising sweeping another  
2     portion of the variable impedance linearly for each impedance setting resulting from  
3     adjusting at least a portion of the variable impedance in increasing increments around  
4     the initial impedance value.

1           11.    The method as recited in claim 8, wherein the variable impedance is a  
2     capacitance.

1           12.    The method as recited in claim 11 wherein the oscillator circuit is a  
2     tank circuit including an inductive element.

1           13.    The method as recited in claim 7 wherein the oscillator circuit is a ring  
2     oscillator.

1           14.    The method as recited in claim 8 wherein the oscillator circuit is a  
2     voltage controlled oscillator (VCO).

1           15.    The method as recited in claim 1 wherein the predetermined portion of  
2     the clock period is adjacent to a clock edge used to sample the input data stream.

1        16. An integrated circuit comprising:  
2        means for detecting whether transitions of an input data stream fall into a  
3                predetermined portion of a clock period of a clock utilized to sample  
4                the input data stream; and  
5        means for evaluating whether a phase-locked loop (PLL) has recovered a  
6                timing associated with the input data stream according to occurrence of  
7                transitions in the predetermined portion of the clock.

1        17. The integrated circuit as recited in claim 16 means for evaluating  
2        includes means for counting a number of evaluation intervals that have one or more  
3                transitions that fall into the predetermined portion of the clock period, generating a  
4                count thereof and determining if lock is achieved according to the count.

1        18. The integrated circuit as recited in claim 16, further comprising means  
2        for changing an output frequency of a variable oscillator circuit if it is determined that  
3        lock is not achieved.

1        19. A method of acquiring a clock embedded in an input data stream,  
2        comprising varying an output of a variable oscillator until transitions of the input data  
3        stream occurring in a predefined phase zone of a sample clock sampling the input data  
4        stream occur below an acceptable rate.

1        20. The method as recited in claim 19 wherein the acceptable rate is  
2        determined according to a number of evaluation intervals having one or more  
3        transitions occurring in the predefined phase zone.

1        21. The method as recited in claim 19 wherein the output of the variable  
2        oscillator is varied by varying an impedance of the variable oscillator.

1        22. The method as recited in claim 19 wherein varying the output of the  
2        variable oscillator comprises varying at least one of a control voltage and a control  
3        current supplied to the variable oscillator.

1        23. An integrated circuit for receiving an input data stream and locking to  
2 a clock embedded in the input data stream using a phase-locked loop, the integrated  
3 circuit comprising:

4              a phase zone detect circuit coupled to determine if a transition of the input data  
5 stream occurs in a predetermined phase zone of a sample clock used to  
6 sample the input data stream;  
7              a counter circuit coupled to the phase zone detect circuit to supply an  
8 indication of a number of evaluation intervals in which at least one bit  
9 error occurs;  
10          a compare circuit coupled to compare the indication and a threshold value and  
11 to output a compare indication, thereby indicating if the phase-locked  
12 loop has locked to the input data stream;  
13          a variable oscillator circuit forming part of the phase-locked loop; and  
14          a control circuit, responsive to the indication that lock is not achieved, to vary  
15 the output of the variable oscillator circuit.

1        24. The integrated circuit as recited in claim 23 wherein:

2              the phase zone detect circuit includes a first data path and a second data path  
3              coupled to receive the input data stream, one of the first and second  
4              data paths being delayed with respect to the other, thereby defining the  
5              phase zone, and wherein an output signal supplied from the first and  
6              second data paths are coupled to a logic circuit to be logically  
7              compared.

1        25. The integrated circuit as recited in claim 23 wherein the first data path  
2 is a phase detector circuit coupled to provide an indication of phase error between a  
3 recovered clock being used to sample the input data stream and the input data stream.

1        26. The integrated circuit as recited in claim 24 wherein the one of the first  
2 and second data paths is delayed by delaying one of the clock and the data of the input  
3 data stream supplied to the one of the first and second data paths.

1           27. The integrated circuit as recited in claim 23 wherein the second data  
2 path includes one or more selector circuits to select from a plurality of clock  
3 frequencies.

1           28. The integrated circuit as recited in claim 24 wherein the first and  
2 second data paths are logically compared in an exclusive OR circuit.

1           29. The integrated circuit as recited in claim 23 further comprising:  
2           a variable impedance circuit forming part of the variable oscillator circuit; and  
3           wherein the control circuit is responsive to the indication that lock is not  
4           achieved, to vary the variable impedance circuit to thereby adjust the  
5           output of the variable oscillator circuit.

1           30. The integrated circuit as recited in claim 29 wherein the control circuit  
2 adjusts the impedance by changing the impedance to successively above and then  
3 below an initial value to provide a gradually increasing swing around an initial  
4 impedance value.

1           31. The integrated circuit as recited in claim 23 wherein the phase-locked  
2 loop is determined to be locked to the input data stream if the indication from the  
3 count circuit indicates that the number of evaluation intervals in which at least one  
4 transition in a predetermined phase zone occurs is below a predetermined threshold  
5 value.

1           32. The integrated circuit as recited in claim 29, wherein the variable  
2 impedance is a capacitance.

1           33. The integrated circuit as recited in claim 23 wherein the oscillator  
2 circuit is a tank circuit including an inductive element.

1           34. The integrated circuit as recited in claim 23 wherein the oscillator  
2 circuit is ring oscillator.

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1           35.   The integrated circuit as recited in claim 23 wherein the oscillator  
2   circuit is a voltage controlled oscillator (VCO).

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